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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PHAM, LY D	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 08/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/680,878	XUE ET AL.
	Examiner	Art Unit
	Ly D. Pham	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,12-14 and 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14 and 16* is/are allowed.

6)☒ Claim(s) *1-7,12 and 13* is/are rejected.

7)☒ Claim(s) *14 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10-7-03 & 10-15-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Reasons for Allowance*.

DETAILED ACTION

1. Applicant's Amendment filed June 27, 2005 has been entered. Claims 12, 14, and 16 have been amended. Claims 8 – 11 and 15 have been canceled.

Claim Objections

2. Claims 14 and 16 are objected to because of the following informalities:

Lines 11 – 14 of claim 14 disclose the *drains ... coupled with a respective word line* and the *gates ... coupled with a respective program line*. On the contrary, according to fig. 7 of the specification, it is believed that the **gates of the memory cells are coupled with a respective word line** and the **drains coupled with a respective program line**.

Appropriate correction is required. Examination will be in accordance with fig. 7 and the specification.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 – 7, 12, and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin et al. (US Pat 6,850,440 B2).

Regarding **claims 1, 6, 7, and 12**, Lin et al. disclose a method for programming a single bit nonvolatile memory cell comprising a semiconductor substrate (figs. 4, 5, 7, or 8, P-substrate) including a source (fig. 4B, source 122), a drain (fig. 4B, drain 114), and a channel in between the source and the drain; and a control gate that comprises a gate electrode (fig. 4B, gate electrode 116) and a dielectric stack (fig. 4B, layer 124 and the top and bottom dielectric layers over above and below layer 124. See also col. 6, lines 38 – 49, col. 8, lines 36 – 47. Dielectric stack being the Oxide-Nitride-Oxide layer), the gate electrode being separated from the channel by the dielectric stack (fig. 4B), the dielectric stack comprising at least one charge storage dielectric layer (fig. 4B, layer 124), wherein the method for programming (col. 3, table 2, under conventional CHISEL programming voltages) comprises:

applying electrical ground to the source (Vsource = 0 Volts);

applying a first voltage having a first polarity to the drain (Vdrain = 1.1 to 3.3 Volts);

applying a second voltage of the first polarity to the control gate (Vcg = 3 to 5 Volts);

applying a third voltage having a second polarity opposite to the first polarity to the semiconductor substrate (Vpwell/psub = -0.5 to –4 Volts),

wherein the first, second, and third voltages cooperatively effect programming of the memory cell as a result of injection of hot carriers generated by a secondary impact

ionization mechanism, the hot carriers being injected into the at least one charge storage dielectric layer from a drain side of the memory cell (col. 1, lines 31 – 42 and line 66 – col. 2, line 4, and lines 52 – 58. See also col. 3, line 15 – col. 4, line 13).

Regarding **claims 2 and 13**, Lin et al. also show the method of claim 1, wherein absolute values of each of the first, second, and third voltages are 5V or less (see table 2, where all applied voltages have absolute values of 5 volts or less).

Regarding **claim 3**, Lin et al. also show the method of claim 1, wherein a difference of absolute values of any two voltages of the first, second, and third voltages is 1.5V or less (see table 2).

Regarding **claim 4**, Lin et al. also show the method of claim 1, wherein an effective gate-to-substrate voltage applied by the second and third voltage is at least 4V (if Vcg is 3V and Vpwell/psub is -1V, the effective Vgate-substrate is 4V).

Regarding **claim 5**, Lin et al. also show the method of claim 4, wherein absolute values of each of the second and third voltages are 5V or less (see above, Vgate-substrate is 4V, which is less than 5V).

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 – 7, 12, and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Bude et al. (US Pat 5,838,617).

Regarding **claims 1, 2 and 12**, Bude et al. disclose a method for programming a single bit nonvolatile memory cell comprising a semiconductor substrate (fig. 1, substrate 30) including a source (fig. 1, source 50), a drain (fig. 4B, drain 70), and a channel in between the source and the drain (fig. 1, channel 80); and a control gate that comprises a gate electrode (fig. 1, gate electrode 40) and a dielectric stack (fig. 1, layers 20, 10, and 60), the gate electrode being separated from the channel by the dielectric stack (fig. 1, gate electrode 40 separated from channel 80 by layers 20, 10, and 60), the dielectric stack comprising at least one charge storage dielectric layer (fig. 1, layer 10), wherein the method for programming (col. 3, lines 30 – 67) comprises:

applying a first voltage having a first polarity to the drain (drain-source bias voltage V_{DS} less than about 5 Volts);

applying a second voltage of the first polarity to the control gate (control gate-source bias voltage V_{CS} of about 10 volts or less. See also col. 10, lines 17 – 26);

applying a third voltage having a second polarity opposite to the first polarity to the semiconductor substrate ('negative substrate-source bias voltage V_{BS} of about –0.5 to –4 volts);

applying electrical ground to the source (since all voltages are with respect to the source, inherently, the source acts as reference potential and is virtually at ground),

wherein the first, second, and third voltages cooperatively effect programming of the memory cell as a result of injection of hot carriers generated by a secondary impact ionization mechanism, the hot carriers being injected into the at least one charge storage dielectric layer from a drain side of the memory cell (col. 3, lines 31 – 48).

Regarding **claim 3**, Bude et al. also disclose the method of claim 1, wherein a difference of absolute values of any two voltages of the first, second, and third voltages is 1.5 V or less (within the ranges disclosed, if V_{DS} is 4.5 volts and V_{BS} is –4volts, the difference of absolute values of these two voltates is 0.5 volts, which is 1.5V or less).

Regarding **claim 4**, Bude et al. also disclose the method of claim 1, wherein an effective gate-to-substrate voltage applied by the second and the third voltages is at least 4 V (again, within the allowable ranges disclosed, if V_{BS} is –3 Volts and V_{CS} is set at 1V, the effective gate-to-substrate voltage is 4V).

Regarding **claim 5**, Bude et al. also disclose the method of claim 4, wherein absolute values of each of the second and third voltages are 5V or less (see above for the exemplary condition where effective gate-to-substrate voltage is 4V, which is 5V or less).

Regarding **claim 6**, Bude et al. further disclose the method of claim 1, wherein the charge storage dielectric layer is positioned between two oxide layers (col. 1, lines 36 – 52, wherein 20 and 60 are the two insulator layers).

Regarding **claim 7**, the feature in which the charge storage dielectric layer comprises nitride is considered inherent in an EPROM or an EEPROM.

Regarding **claim 13**, since Bude et al. have shown all applied bias voltages each having an absolute value of 5V or less, therefore, it is considered inherent that the peripheral circuitry comprises circuitry for generating an on-chip voltage having an absolute value of 5V or less.

Allowable Subject Matter

6. Claims 14 and 16 are allowed.

7. The following is an examiner's statement of reasons for allowance:

The prior arts teach a memory circuit, comprising:

an array of single bit nonvolatile memory cells organized in columns, wherein each of the memory cells comprises a substrate, a source, a drain, a channel, and a control gate that comprises a gate electrode and a dielectric stack, and the dielectric stack comprising at least one charge storage dielectric layer, wherein

adjacent memory cells in each column of the memory circuit have one of their sources and drains in common;

the gates of the memory cells in each column are coupled with a respective word line, ...

However, the prior arts did not disclose the memory circuit, further comprising:

the sources of the memory cells in each column ... are coupled with the same bit line, ...;

the drains of the memory cells in each column ... are coupled with a respective program line, ...; and

wherein programming a memory cell of the memory circuit comprises, in combination:

applying electrical ground to a first bit line;

applying a first voltage having a first polarity to a word line;

applying a second voltage of the first polarity to a program line;

applying a third voltage, having a second polarity opposite to the first polarity to the semiconductor substrate; and

applying a fourth voltage of the first polarity to all other bit lines ....

8. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

10. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02(b)).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly D. Pham whose telephone number is 571-272-1793. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ly Pham
August 9, 2005

HUAN HOANG
PRIMARY EXAMINER